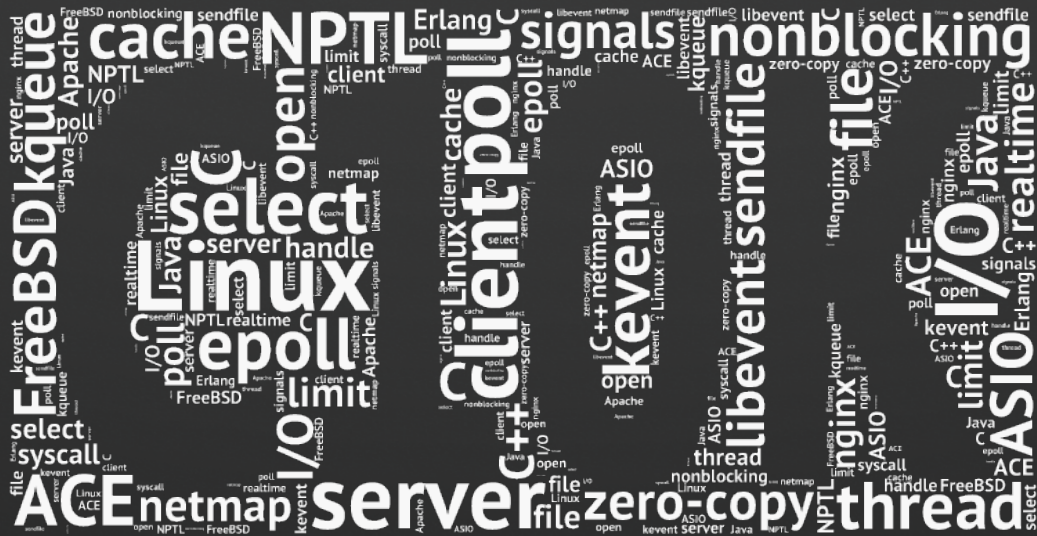




从C10K到C10M

高性能网络的探索与实践



C10K Killer

Model

blocking/nonblocking

synchronous/asynchronous

multiplexing

Implement

epoll/kqueue/iocp

Then

Framework

libevent/libev/boost::asio

Software

nginx/haproxy/squid



More Performance

CPU Affinity & Data Locality

RPS/RFS/RSS/

XPS

IRQ Tuning

Kernel Tuning

CPU Affinity & Data Locality

`sched_set_affinity()`

or

`taskset/numactl`

RPS/RFS/RSS/ XPS

RPS – Receive Packet Steering

RFS – Receive Flow Steering

RSS – Receive Side Scaling (hardware)

XPS – Transmit Packet Steering

IRQ Tuning

Interrupt Coalescing

NAPI/Newer newer NAPI

SMP IRQ Affinity

```
echo $bitmask > /proc/irq/{#}/smp_affinity
```

Kernel Tuning

Offload

TSO/GSO LRO/GRO

Kernel Parameter

net.ipv4.tcp_*/net.core.*

Next, we talk
about ..

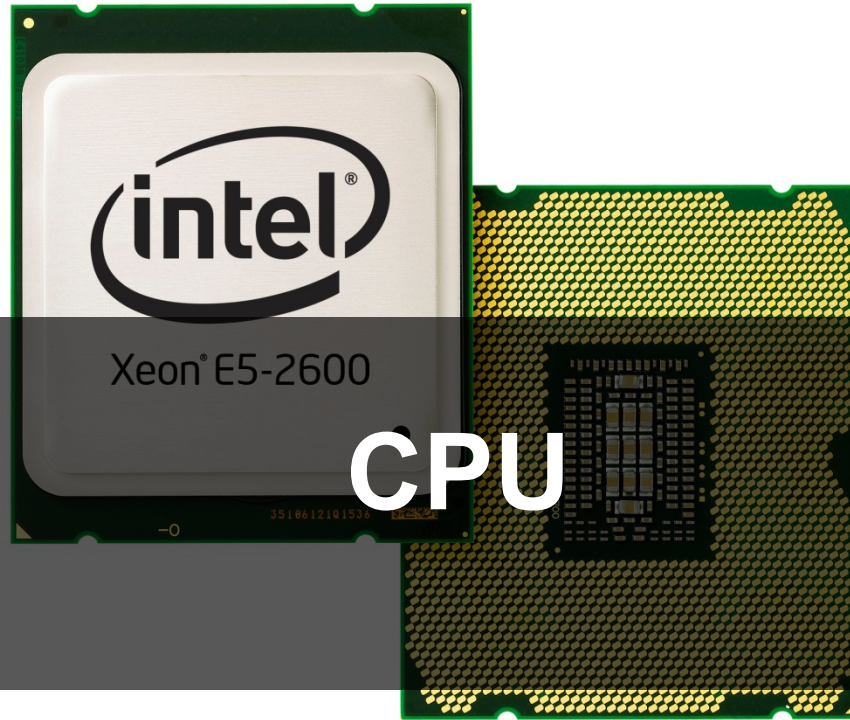


Hardware

OS

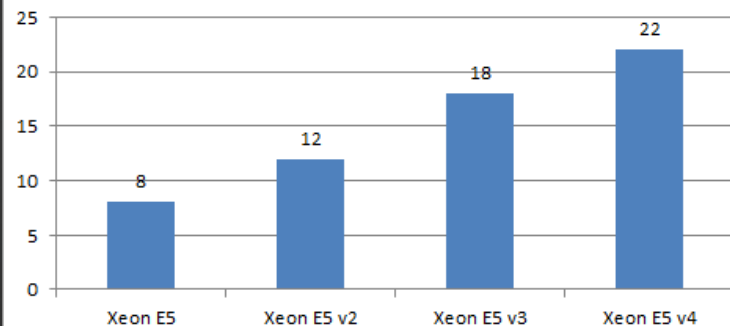
Application

Modern Hardware

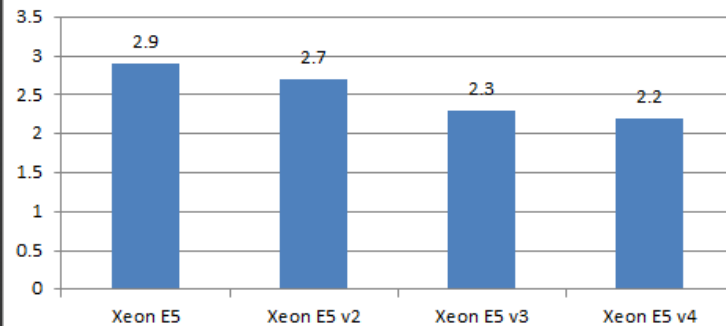


CPU

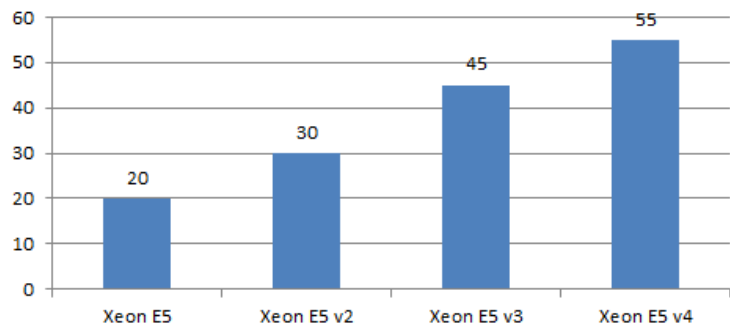
**Intel Xeon E5-2600 Series
Cores**



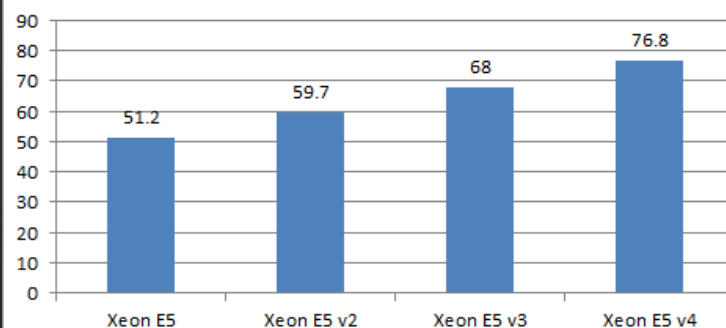
**Intel Xeon E5-2600 Series
Frequency(MHz)**

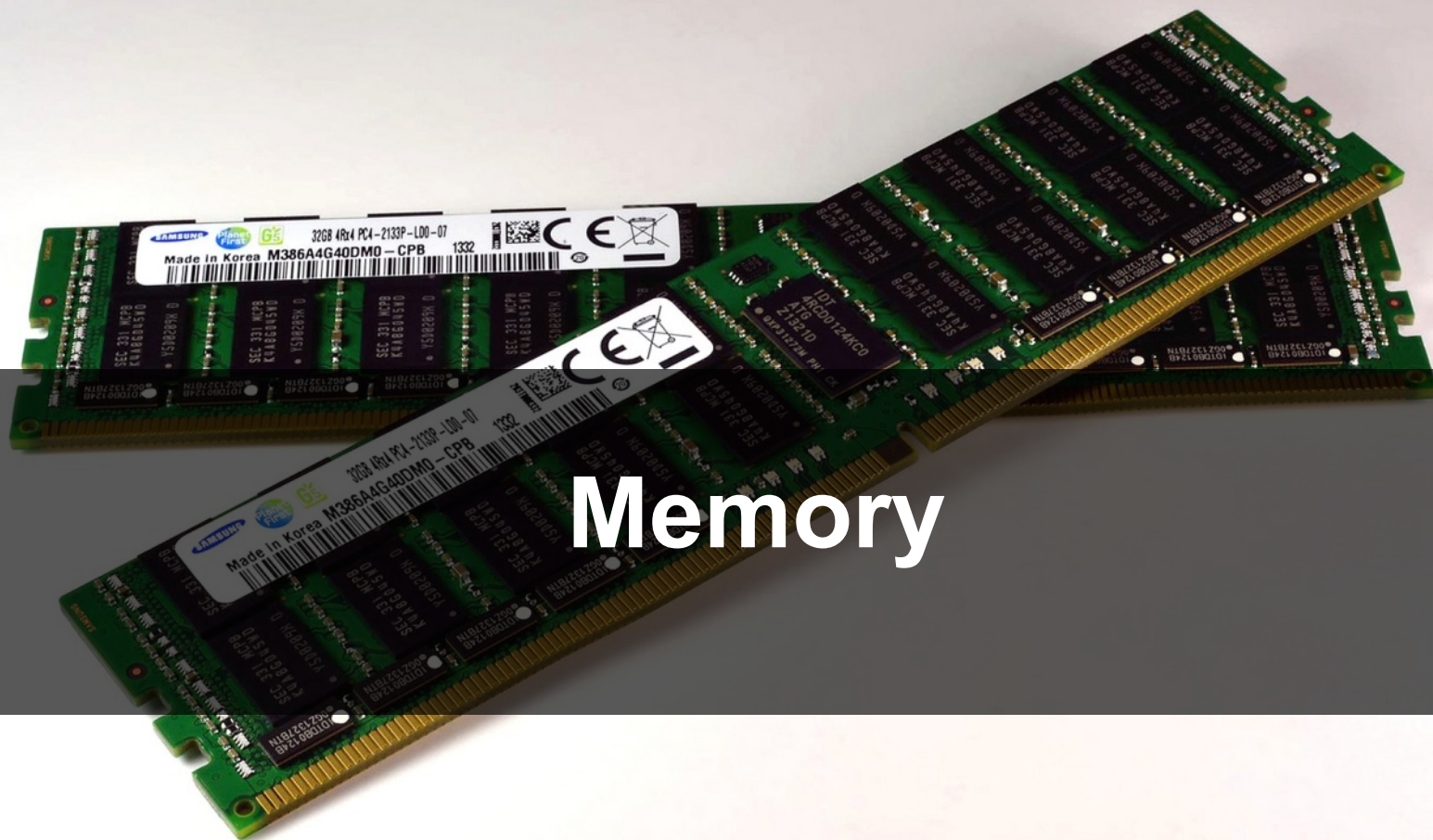


**Intel Xeon E5-2600 Series
L3 Cache(MB)**



**Intel Xeon E5-2600 Series
Memory Bandwidth(GB/s)**





Memory

DDR4 Transition by Segment



Technology Forecast

- Mobile DRAM share was down slightly in Q1-15
 - 32% of bits shipped in Q1-15 were mobile DRAM (from 34% in Q4-14)
 - Expected to settle at 45%-50% on annual basis
 - Back quarterly share will exceed 50%

Servers: full support in 2014

- Small DDR4 volumes in 1H 2014 – validation phase
- Volumes picked up in 2H 2014
- >50% adoption by end of 2015

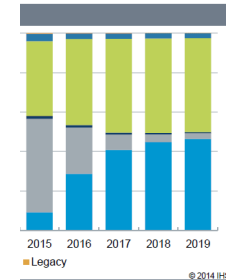
Upcoming Intel® Platforms Continue to Support DDR4



Intel® Xeon® Processor E5-2600 v4 product family support DDR4 up to 2400.



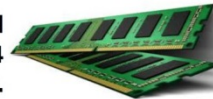
2015



Mainstream PCs now supporting DDR4, 6th Generation Intel® Core™ processor 6000 series now supporting DDR4 up to 2133.



Memory Ecosystem ready for DDR4 on future Intel Xeon and Intel Core Processor Extreme Editions. Inquire about DDR4 availability and pricing through your preferred memory vendor.



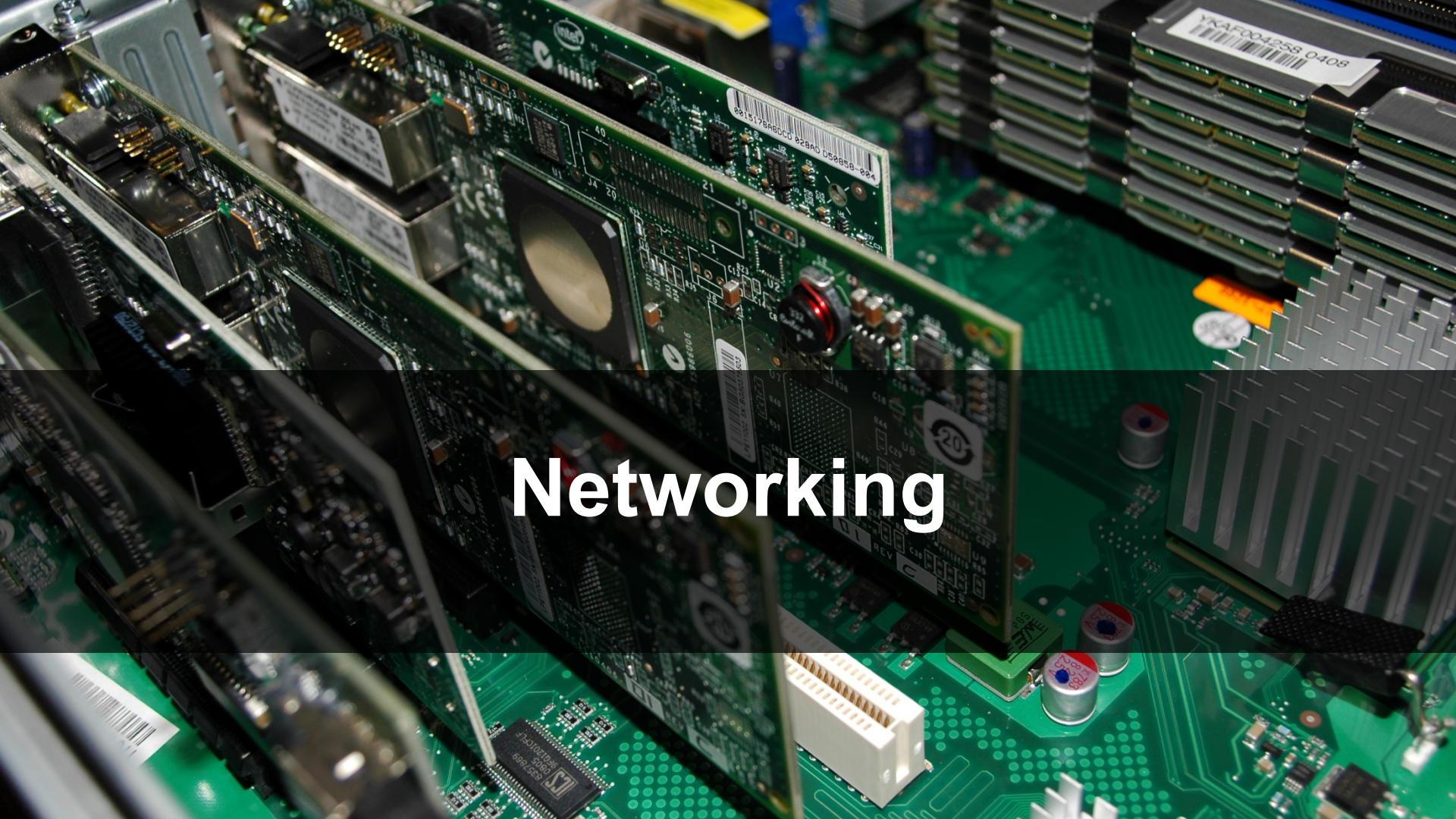
Desktops: minor support

2014, widespread in 2015

Small DDR4 penetration in 2H 2014

Adoption ramps quickly in 2016





Networking

Intel® Ethernet Controllers and PHYs

Product	Codename	Device	Package Size/ Physical Package	Host Interface/ Bus Type	Performance Features
10/40 GbE Silicon					
Intel® XL710-AM2 	Fortville	Dual Port 40GbE MAC/PHY, KR4/CR4/XLAUI/XLPPI, KR/SFI/XAUI, KX4/KX/SGMII	25x25 mm 576-pin Flip-Chip	PCI Express® v3.0 (8.0 GT/s) x8/x4/x1	1536 queue pairs in the device and 16 per virtual function, 128 VFs for the device, 384 VSI in the device. VXLAN, NVGRE and Geneve stateless offloads, Intel(r) Ethernet Flow Director, Optimized for Intel(r) Data Plane Developer Kit for small packet performance, FCoE CRC offload, FCoE direct data placement
Intel® XL710-AM2 	Fortville	Single Port 40GbE MAC/PHY, KR4/CR4/XLAUI/XLPPI, KR/SFI/XAUI, KX4/KX/SGMII	25x25 mm 576-pin Flip-Chip	PCI Express® v3.0 (8.0 GT/s) x8/x4/x1	1536 queue pairs in the device and 16 per virtual function, 128 VFs for the device, 384 VSI in the device. VXLAN, NVGRE and Geneve stateless offloads, Intel(r) Ethernet Flow Director, Optimized for Intel(r) Data Plane Developer Kit for small packet performance, FCoE CRC offload, FCoE direct data placement
Intel® X710-AM2 	Fortville	Single Port 40GbE MAC/PHY, KR4/CR4/XLAUI/XLPPI, KR/SFI/XAUI, KX4/KX/SGMII	25x25 mm 576-pin Flip-Chip	PCI Express® v3.0 (8.0 GT/s) x8/x4/x1	1536 queue pairs in the device and 16 per virtual function, 128 VFs for the device, 384 VSI in the device. VXLAN, NVGRE and Geneve stateless offloads, Intel(r) Ethernet Flow Director, Optimized for Intel(r) Data Plane Developer Kit for small packet performance, FCoE CRC offload, FCoE direct data placement
Intel® X540-AT2 Intel® X540-BT2 	Twinville	Dual Port 10GbE MAC/PHY, 10GBase-T, 1000Base-T, 100Base-T	25x25 mm 576-pin Flip-Chip	PCI Express® v2.1 (5.0 GT/s) x8/x4/x2/x1	128 Tx and 128 Rx queues, Receive Side Coalescing (RSC), low latency interrupts, Intel® Ethernet Flow Director, Intel® Virtualization Technology for Connectivity (Intel® VT-c) (VMDq, SR-IOV), FCoE CRC offload, FCoE direct data placement
Intel® 82599ES 	Niantic	Dual Port 10GbE MAC/PHY, KR, SFI, XAUI, KX/KX4, CX4, BX, SGMII	25x25 mm 576-pin Flip-Chip	PCI Express® v2.0 (5.0 GT/s) x8/x4/x2/x1	128 Tx and 128 Rx queues, Receive Side Coalescing (RSC), low latency interrupts, Intel® Ethernet Flow Director, Intel® Virtualization Technology for Connectivity (Intel® VT-c) (VMDq, SR-IOV), FCoE CRC offload, FCoE direct data placement
Intel® 82599EB 	Niantic	Dual Port 10GbE MAC/PHY, XAUI, KX/KX4, CX4, BX, SGMII	25x25 mm 576-pin Flip-Chip	PCI Express® v2.0 (5.0 GT/s) x8/x4/x2/x1	128 Tx and 128 Rx queues, Receive Side Coalescing (RSC), low latency interrupts, Intel® Ethernet Flow Director, Intel® Virtualization Technology for Connectivity (Intel® VT-c) (VMDq, SR-IOV), FCoE CRC offload, FCoE direct data placement
Intel® 82599EN 	Niantic	Single Port 10GbE MAC/PHY, SFI	25x25 mm 576-pin Flip-Chip	PCI Express® v2.0 (5.0 GT/s) x8/x4/x2/x1	64 Tx and 64 Rx queues, Receive Side Coalescing (RSC), low latency interrupts, Intel® Ethernet Flow Director, Intel® Virtualization Technology for Connectivity (Intel® VT-c) (VMDq, SR-IOV), FCoE CRC offload, FCoE direct data placement



We are ready!



We are ready!
But...

Packet Processing

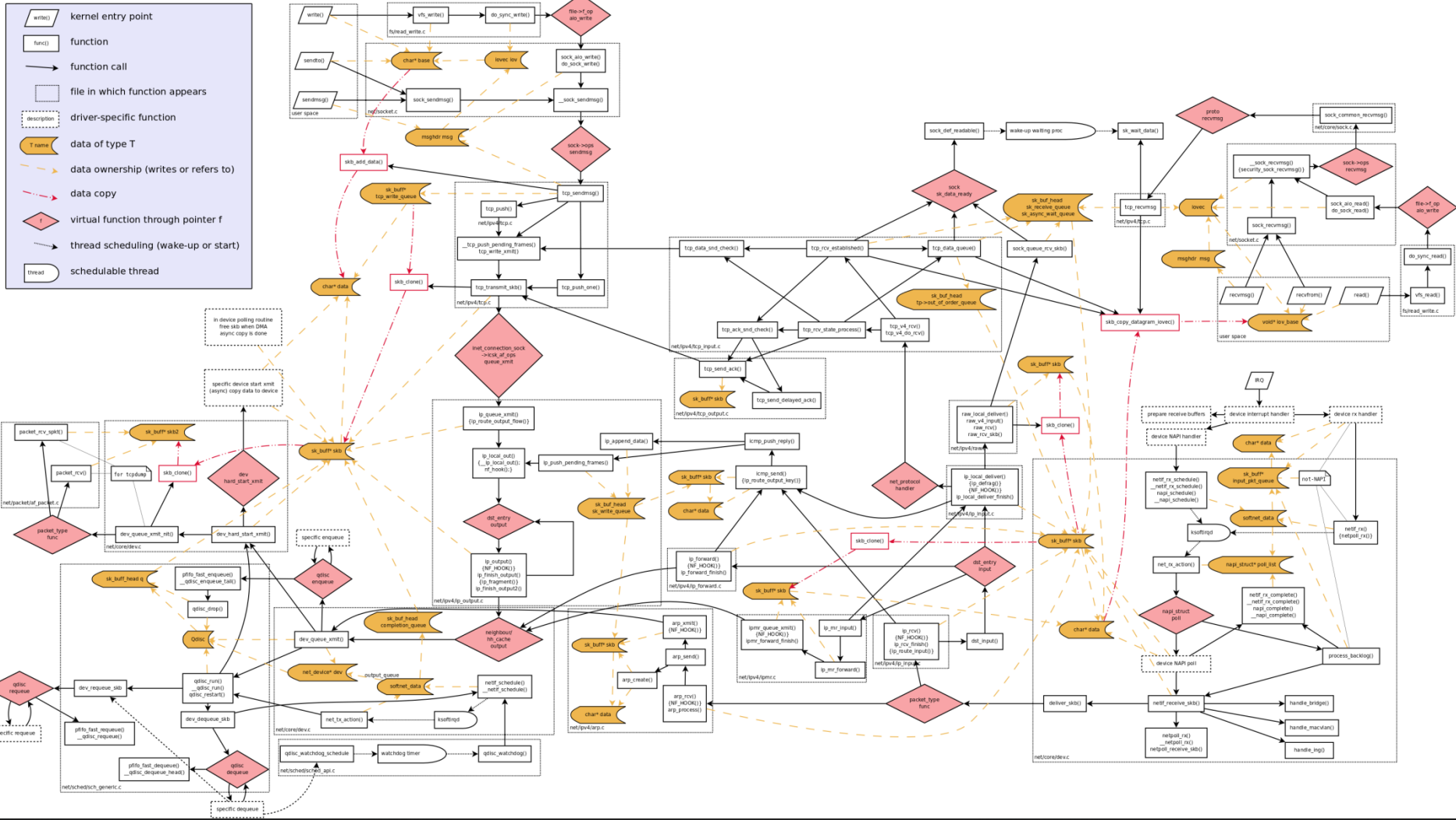
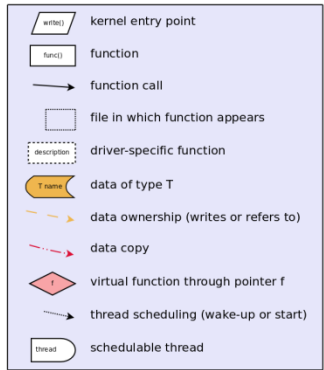
Task Scheduling

Data Access

The kernel isn't the solution.

The kernel is the **problem**.

- Shmoocon 2013



Global accept queue ☹️

Global established table ☹️

Optimize networking stack 😊

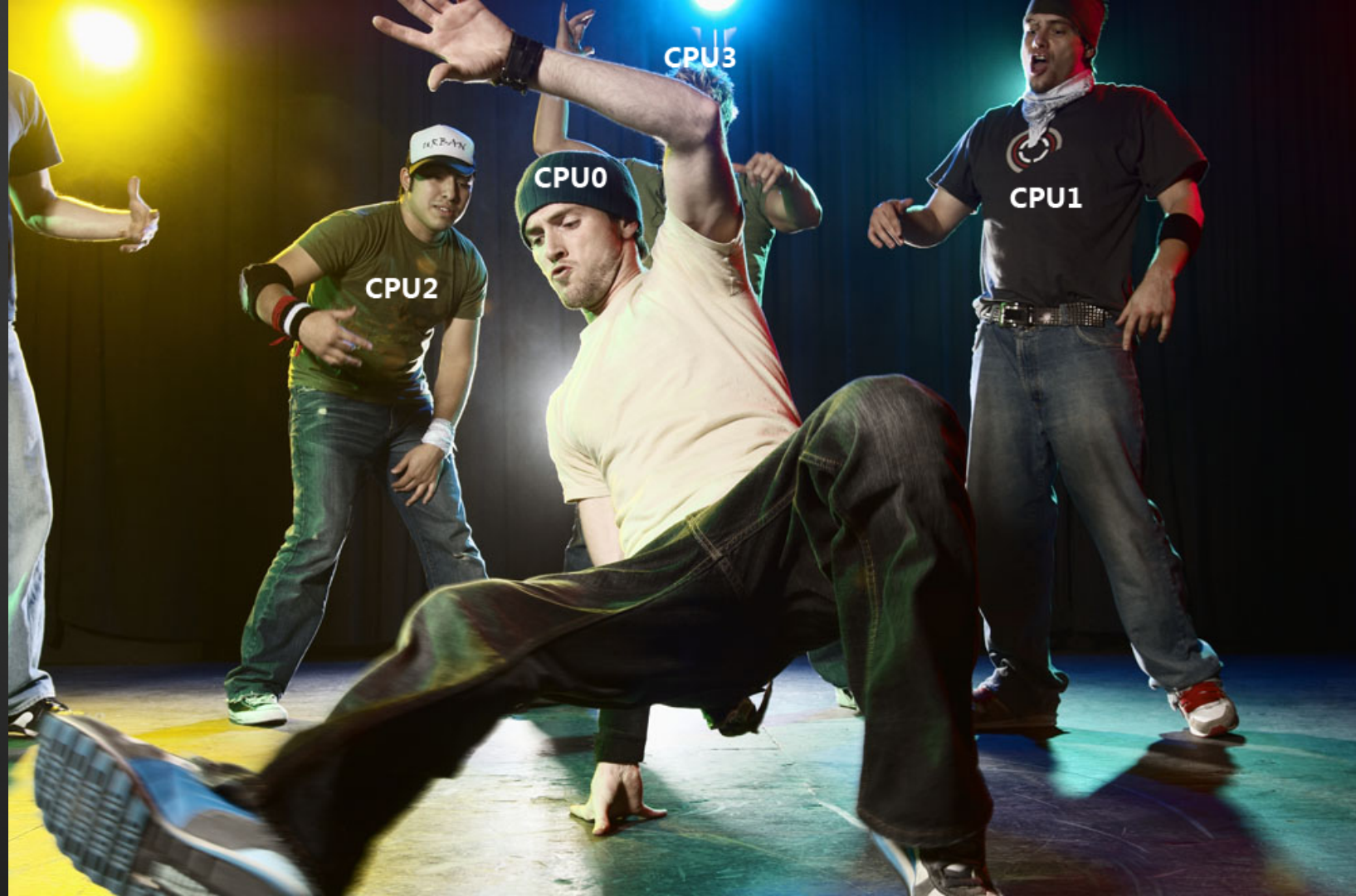
Move networking stack to userspace 😊

Hook networking stack 😊

Userspace I/O 😊

Raw Packets?

Maybe I need a protocol stack.



Multiple process/thread

!=

Multiple core

Connection locality 😊

Lockless data structures 😊

Keep data structures per core 😊

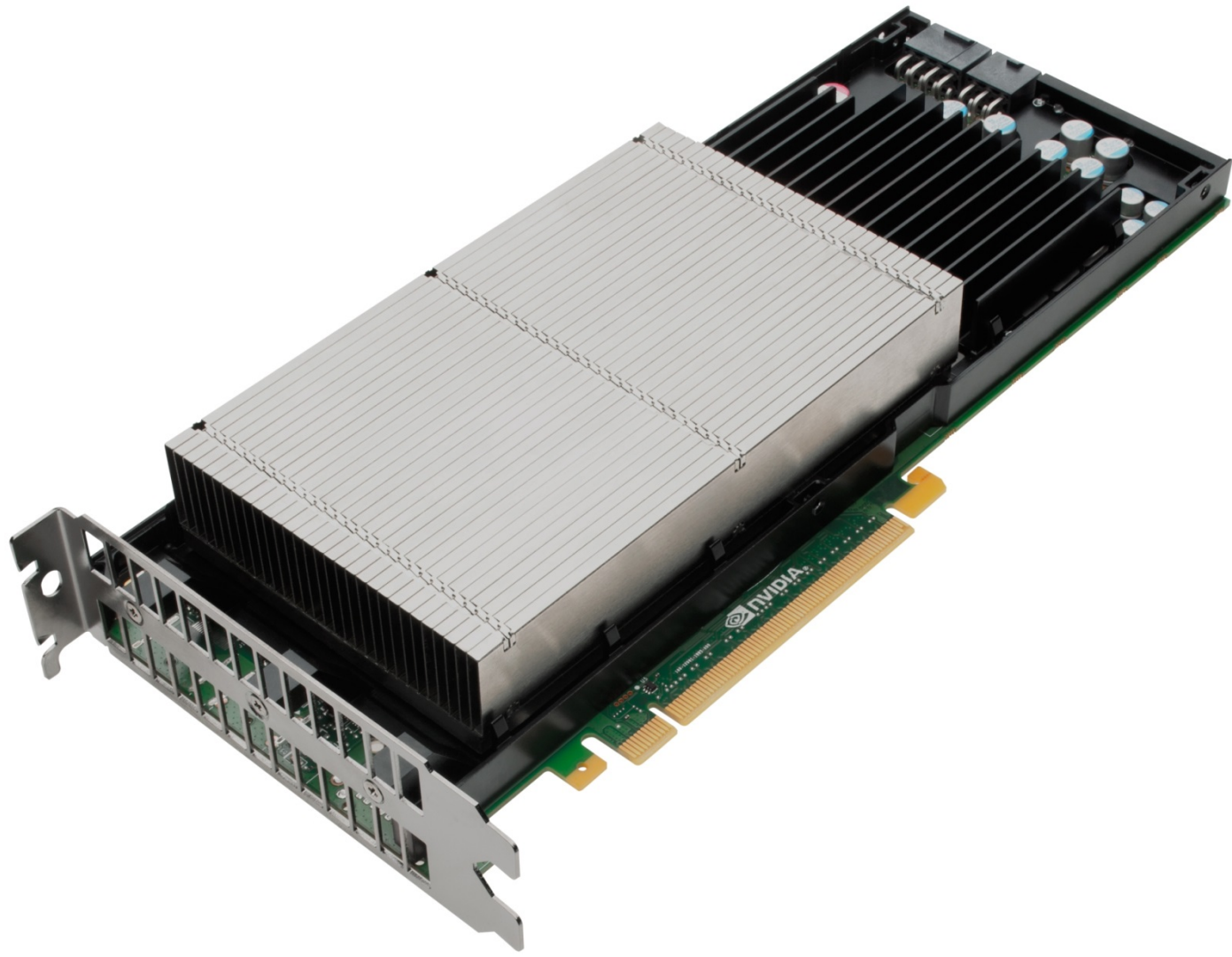
Latency Comparison Numbers

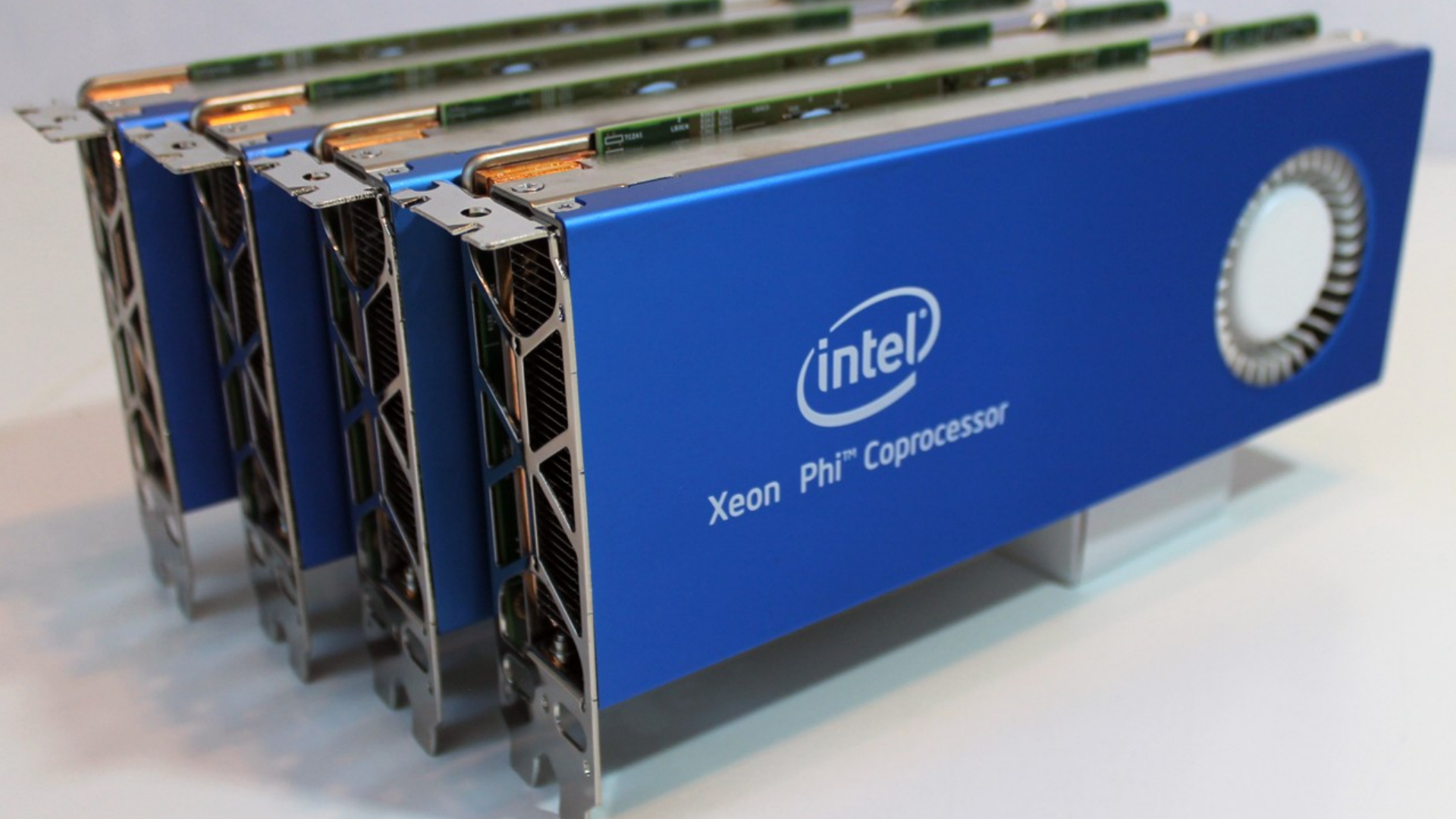
Latency Comparison Numbers		
Register/Buffer reference	0.4 ns	(1 cycle)
L1 cache reference	1.6 ns	(4 cycles)
L2 cache reference	4.8 ns	(12 cycles)
L3 cache reference	10.4 ns	(26 cycles)
Linux SYS_gettid syscall	50.0 ns	
Main Memory reference	61.0 ns	
Process context switches with CPU affinity	1000.0 ns	
Process context switches without CPU affinity	1300.0 ns	
Send 1K bytes over 1 Gbps network	10000.0 ns	
Read 4K randomly from SSD	150000.0 ns	
Read 1 MB sequentially from memory	250000.0 ns	
Round trip within same datacenter	500000.0 ns	
Read 1 MB sequentially from SSD	1000000.0 ns	
CPU: Intel(R) Core(TM) i7-5500U CPU @ 2.40GHz		
RAM: 8 GB (Double PC3L-12800 11-11-11-28)		

No nested pointer 😊

Hugepages 😊

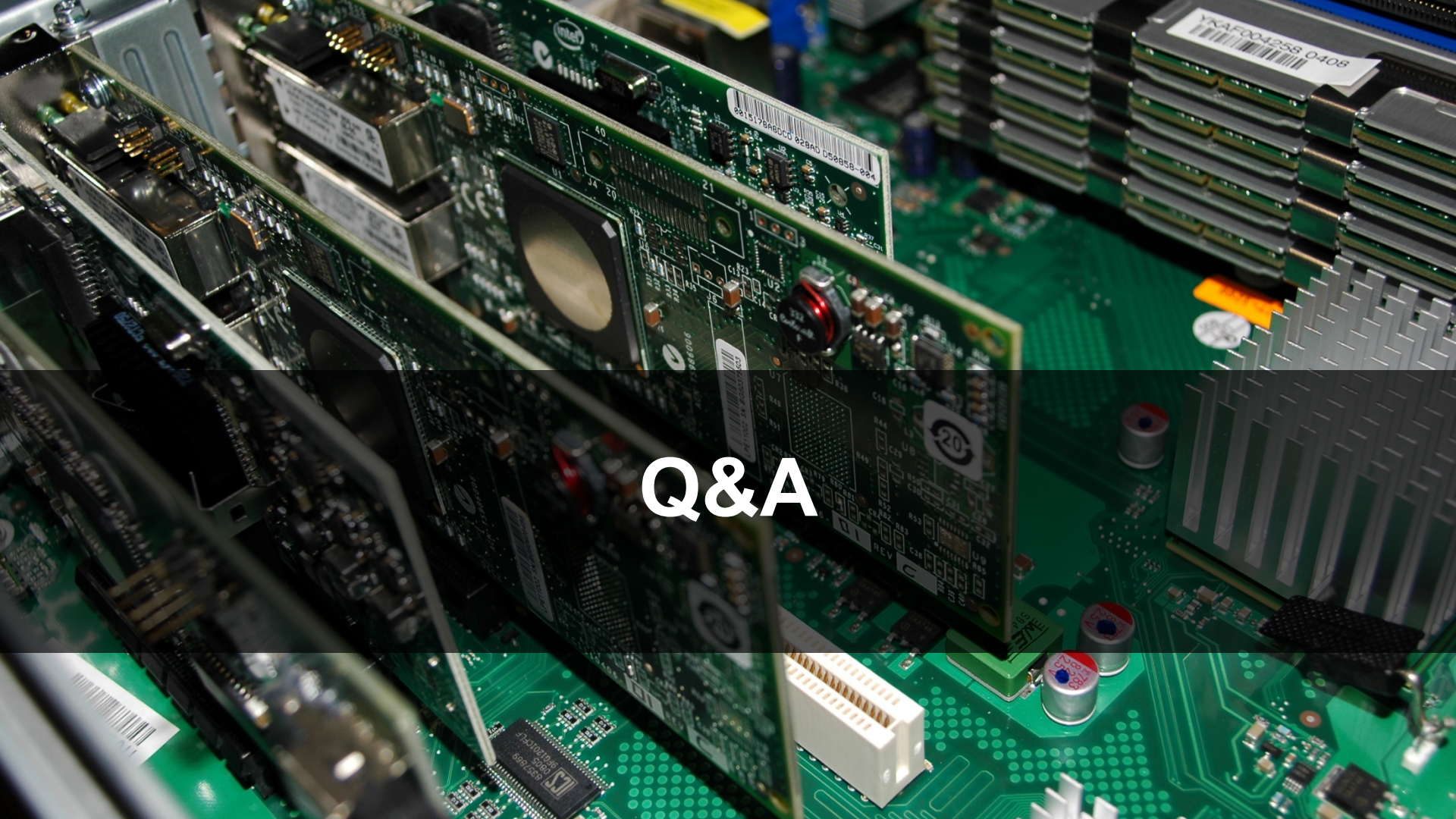
Preallocate memory 😊





The image shows a row of Intel Xeon Phi coprocessor modules. Each module has a blue front plate with the Intel logo and the text 'Xeon Phi™ Coprocessor'. The modules are connected to a green circuit board with gold-plated contacts. A circular fan is visible on the right side of the front plate.

intel
Xeon Phi™ Coprocessor



Q&A